Si9706DY

PC Card (PCMCIA) Interface Switch

Features

- Single SO-8 Package
- CMOS-Logic Compatible Inputs
- Slow V_{CC} Ramp Time
- Smart Switching
- Extremely Low R_{ON}
- Reverse Blocking Switches
- Low Power Consumption
- Safe Power Up

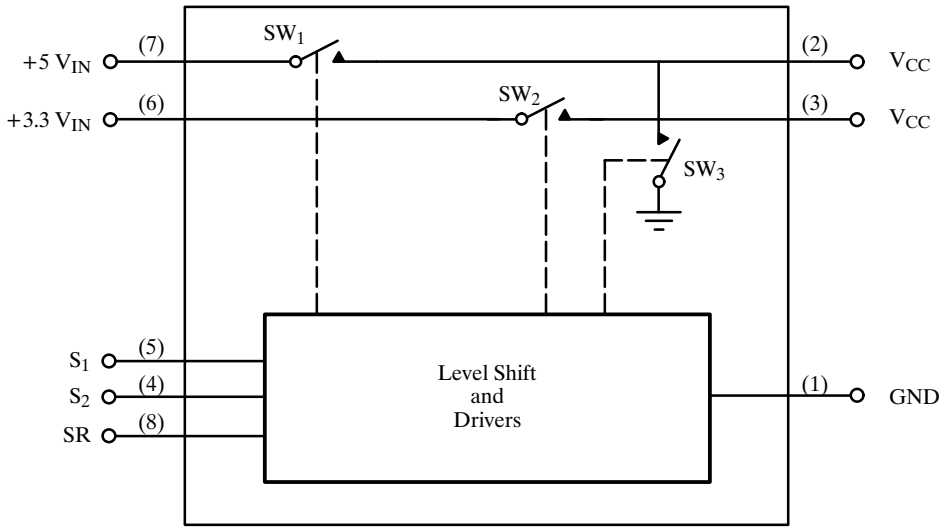
Description

The Si9706DY offers an integrated solution for PC Card power interfaces that only require V_{CC} switching. This part is ideal for systems that operate at 5 V and provide V_{PP} from the main supply or from a dedicated Flash RAM 12-V supply.

The Si9706DY operates off the 5-V supply and has built-in level shifting for gate drive. Internal logic protects against a control logic error that would short 5 V to the 3.3-V supply. This protection logic also allows the Si9706DY to be configured for positive or negative control logic for compatibility with a variety of PC Card controllers. These control inputs are CMOS logic compatible and can be driven to 3.3 V or 5 V.

The Si9706DY PC Card interface switch is packaged in a narrow body SO-8 package and is rated over the industrial temperature range −40 to 85°C.

Functional Block Diagram



Absolute Maximum Ratings

Voltages Referenced to Ground
+5 V_{IN} ..... 7 V
+3.3 V_{IN} ..... 7 V
S_1, S_2 (CMOS Inputs) ..... 7 V
All Pins ..... −0.5 V
I_{OUT} V_{CC}[a] ..... 4 A
PD Max[b]: (T_A = 25°C) ..... 1.59 W
(T_A = 85°C) ..... 0.63 W

Junction Temperature ..... 125°C
Thermal Ratings[b]: $R_{\Theta JA}$ ..... 63 °C/W

Notes
a. Pins 2, 3 connected together externally.
b. Mounted on 1-IN^2, FR4 PC Board.

Recommended Operating Conditions

+5 V_{IN} (must be present) ..... 5 V ±10%
+3.3 V_{IN} ..... 3.3 V ±10%
C_{SR} ..... 33 nF
I_{OUT} V_{CC}[a] ..... 2 A

V_{CC} Load Capacitance ..... 150 µF Max

Notes
a. Pins 2, 3 connected together externally.

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified C_{SR} = 33 nF, +5 V_{IN} = 5 V +3.3 V_{IN} = 3.3 V, Low ≤ 0.8 V, High ≥ 2.2 V		Limits −40 to 85°C Min[a]	Typ[b]	Max[a]	Unit
Switch SW_1							
On-Resistance	R_{ON}	I = 500 mA, S_1 = High S_2 = Low	T_A = 25°C		58	70	mΩ
			T_A = 85°C		73	90	
Off Current (V_{CC})	I_{OFF}	+5 V_{IN} = 5.5 V, V_{CC} = 0 V S_1 = S_2 = Low	T_A = 25°C			1	µA
			T_A = 85°C			10	
Rise Time	$t_{S1(on)}$	S_2 = Low, See Figure 1		0.2	1.7	5	ms
Fall Time	$t_{S1(off)}$			10	30	50	
Switch SW_2							
On-Resistance	R_{ON}	I = 500 mA, S_2 = High S_1 = Low	T_A = 25°C		44	55	mΩ
			T_A = 85°C		55	70	
Off Current (+3.3 V_{IN})	I_{OFF}	+3.3 V_{IN} = 3.6 V, V_{CC} = 0 V S_1 = S_2 = Low	T_A = 25°C			1	µA
			T_A = 85°C			10	
Rise Time	$t_{S2(on)}$	S_1 = Low, See Figure 1		0.1	0.9	5	ms
Fall Time	$t_{S2(off)}$			5	20	40	
Switch SW_3							
On-Resistance	R_{ON}	I = 2 mA, S_1 = S_2 = Low	T_A = 25°C		140	400	Ω
			T_A = 85°C		200	500	
Power Supply							
+5 V_{IN} Current Input (on)	$I_{+5VIN(1)}$	S_1 = 0 V, S_2 = 3 V			20	50	µA
	$I_{+5VIN(2)}$	S_1 = 3 V, S_2 = 0V			20	50	
+5 V_{IN} Current Input (off)	$I_{+5VIN(3)}$	S_1 = S_2 = 0 V			< 1	10	

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified C_{SR} = 33 nF, +5 V_{IN} = 5 V +3.3 V_{IN} = 3.3 V, Low ≤ 0.8 V, High ≥ 2.2 V	Limits −40 to 85°C Min[a]	Typ[b]	Max[a]	Unit
Switch Control Inputs S_1, S_2						
Input Voltage High	$V_{I(H)}$	+5 V_{IN} = 5.5 V	2.2	1.8		V
		+5 V_{IN} = 4.5 V	2.2	1.6		
Input Voltage Low	$V_{I(L)}$	+5 V_{IN} = 5.5 V		1.6	0.8	
		+5 V_{IN} = 4.5 V		1.4	0.8	
Input Current High	$I_{I(H)}$	S_1, S_2 = 5 V			1.0	µA
Input Current Low	$I_{I(L)}$	S_1, S_2 = GND	−1.0			

Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Timing Waveforms

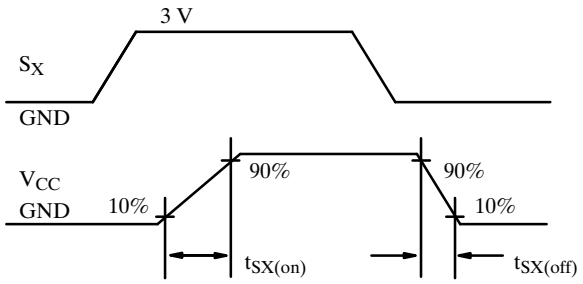


Figure 1. Switch Ramp

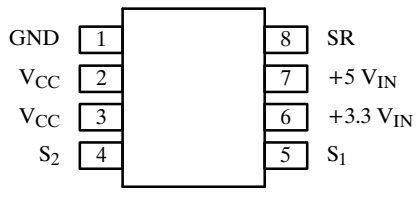
Truth Table

S_1	S_2	Switch 1	Switch 2	Switch 3
0	0	Off	Off	On
0	1	Off	On	Off
1	0	On	Off	Off
1	1	Off	Off	On

Notes
a. Switch 1 and 2 are delayed until after V_{CC} is valid.
b. Shaded line is an error condition for PC Card applications.
c. The smart switching of the Si9706DY avoids potential host damage by defaulting to off during error conditions.

Pin Configuration and Description

SO-8

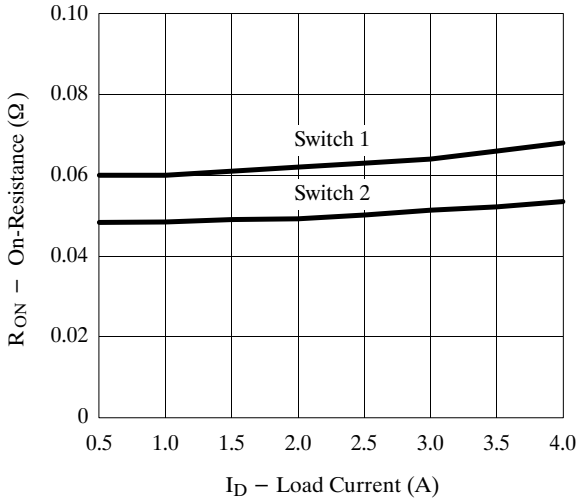


Top View

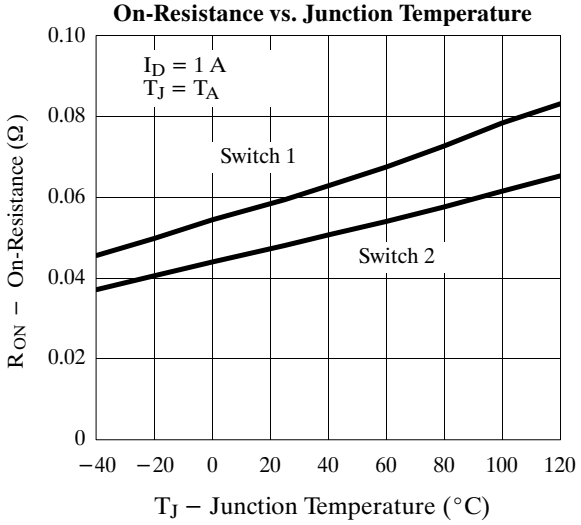
Function	Pin Number	Description
S_1	5	Control input for selecting +5 V_{IN} to V_{CC}.
S_2	4	Control input for selecting +3.3 V_{IN} to V_{CC}.
GND	1	Ground connection.
V_{CC}	2, 3	Supply voltage to slot.
+3.3 V_{IN}	6	+3.3-V supply.
+5 V_{IN}	7	+5-V supply.
SR	8	Slew rate control pin.

Typical Characteristics (25°C Unless Otherwise Noted)

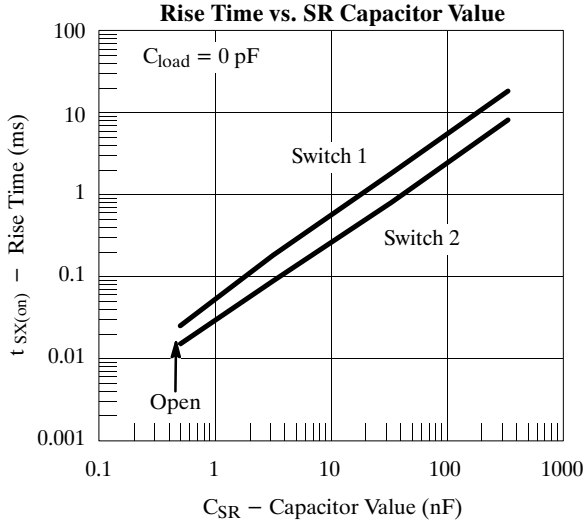
On-Resistance vs. Load Current



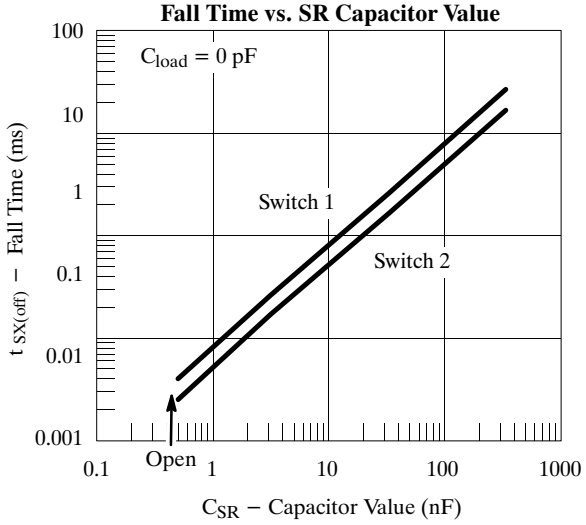
On-Resistance vs. Junction Temperature



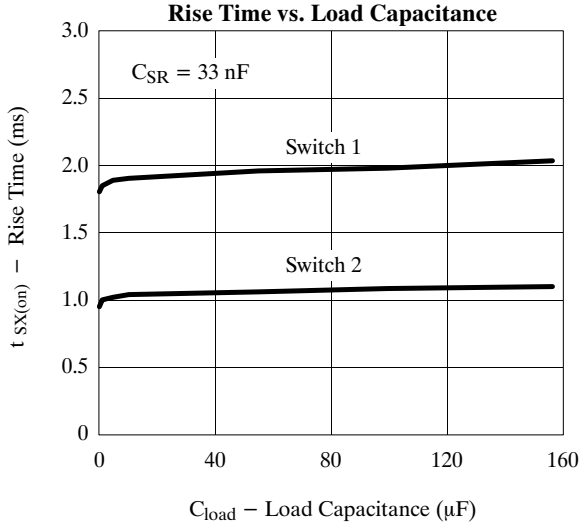
Rise Time vs. SR Capacitor Value



Fall Time vs. SR Capacitor Value



Rise Time vs. Load Capacitance



Fall Time vs. Load Capacitance